

**ABSTRACT**

A method and apparatus for correcting the timing skew of data signals in a parallel data transmission system, such as a Small Computer System Interface (SCSI) data bus, relative to a receive clock in the data bus. The system separately corrects the receive clock duty cycle, and also features independent de-skewing of the rising and falling edges of a data waveform to improve timing accuracy of transmitted signals. The method and apparatus can be used without substantial changes to existing transmission system protocols, and can be implemented on an all-digital integrated circuit.